REMARKS

The Office Action is described in detail below.

Claim Rejections - 35 USC 103

Paragraph 4 of Office Action

Claims 1,7-9 and 16-53 are rejected under 35 USC 103(a) as being unpatentable over Morishita (US 5,529,956) in view of Harshfield (US 6,031,287).

Claim 1 of the present invention recites:

1. A method of making an electrically programmable memory element, comprising:

providing a first dielectric layer, said first dielectric layer having an opening, said opening having a sidewall surface and a bottom surface;

forming a conductive layer on said sidewall surface and said bottom surface;

removing at least a portion of said conductive layer from said bottom surface;

forming a second dielectric layer on said conductive layer within said opening; and

forming a programmable resistance material in electrical communication with said conductive layer.

Morishita is directed to a method of making a multi-layer wiring structure. Referring to Figure 1D, a partial structure of the multi-layer wiring structure is shown. Using an electroplating process, gold is plating-grown in the through hole 8 until the grown gold reaches he same height as a level of a surface of the first conductive film 5. At this process, an electric current for the electroplating is supplied to the first conducting film 5, the second conducting film 10 and the lower level wiring conducting 3. (See Morishita column 4, lines 13-18).

On a semiconductor substrate there is typically an array of structures Figure 1D. Each structure has its own lower level wiring conductor 3 and all of the lower level wiring conductors 3 should be kept at the same potential during the electroplating process to ensure good quality. The second conducting film 10 electrically interconnects the lower level wiring conductor 3 to the first conducting film 5. First conducting film 5 is coupled to another second conducting film 10 (of another structure Figure 1D) which is coupled to another lower level wiring conductor 3. In this manner, during the electroplating process, all of the lower level wiring conductors 3 will be at the same potential.

Hence, the second conducting film 10 is merely used as an electrical interconnect to couple the lower level wiring conductor 3 to the first conducting film 5 to keep the two at the same potential during the electroplating process. After the structure 1G is complete, the second conducting film provides for some small amount of interconnecting between the lower level wiring conductor 3 and the upper level wiring conductor 7. However, the primary conductive pathway between the lower level wiring conductor 3 and the upper level wiring conductor 7 is via the conductive material filling the through hole 8 and not the second conductive film 10.

Hence, in Morishita, the second conductive film 10 is used as an interconnect between two conductors. There is no teaching or suggestion in Morishita that the second conductive film 10 can be used in combination with a programmable resistance memory material to form an electrically programmable memory. More specifically, there is no teaching or suggestion in Morishita that the second conductive film 10 may be used appropriately to provide an electrical energy (e.g. an electrical current) to a programmable resistance memory material in order to program the memory material between its resistance states.

Harshfield is directed to a chalcogenide memory element. One embodiment of Harshfield is shown in Figure 25. In this embodiment, a memory material 124 is coupled between a first conductive layer 106 and a second conductive layer 146. An electrical energy passing between the first conductive layer 106 and the second conductive layer 146 (through the memory material 124) programs the memory material 124. Neither Morishita, Harshfield nor the combination of Morishita and Harshfield provides any teaching or suggestion that the upper level wiring conductor 7 of Morishita may be replaced with a chalcogenide memory material. Neither reference provides any teaching or suggestion that the second conductive film 10 may be used as a programming means to program a chalcogenide material rather than merely as an interconnect means of interconnecting to conductors.

In addition, it is noted that in Harshfield the chalcogenide material 124 is between the first conductive layer 106 and second conductive layer 146. In contrast, in Morishita the second conductive film 10 is between the upper level wiring conductor 7 and lower level wiring conductor 3. Hence, once again, Harshfield provides no teaching or suggestion that the upper level wiring

conductive 7 of Morishita should be replaced with a chalcogenide material.

A second embodiment of Harshfield is shown in Figure 31. In this embodiment a memory material 166 is coupled between a conductive layer 162,164 and conductive layer 168. An electrical energy provided by conductive layer 162,164 programs the memory material. Neither Harshfield, Morishita nor the combination of Harshfield and Morishita provide any teaching or suggestion that the second conducting film 10 of Morishita may be used instead of the conductive layer 162,164 of Harshfield. Once again, there is no teaching that the second conductive film 10 may be used to provide electrical energy to a programmable resistance memory material to program the memory material.

To establish a prima facie case of obviousness there must be some suggestion or motivation to combine reference teachings. In addition, there must be some expectation of success. In the present case, there is no suggestion or motivation to combine references (and there is no expectation of success) such that the second conductive film 10 in Morishita may be used program a programmable resistance material. The rejection of claims 1, 7-9, 16-53 under 35 USC 103(a) as being unpatentable over Morishita in

view of Harshfield is thus improper an applicants request it be removed.

SUMMARY

In view of the above remarks, claims 1 and 7-9, 16-57 are in condition of allowance. Applicants respectfully request reconsideration, withdrawal of the outstanding rejections and notification of allowance. Should the Examiner have any questions or suggestions regarding the prosecution of this application, he is asked to contact applicants' representative at the telephone number listed below.

Respectfully submitted,

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